REMARKS/ARGUMENTS

Brief Summary of Status

Claims 1-24 are pending in the application.

Claims 1-24 are rejected.

35 U.S.C. § 103 (starting page 3 of non-final office action)

The Examiner asserts:

"6. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cherubini et al (US Patent Number 6,741,551) in view of McCallister et al (US 6,005,897)." (hereinafter referred to as "Cherubini" and "McCallister", respectively)(non-final office action, Paper No./Mail Date 20080219, p. 3)

Remarks

35 U.S.C. § 103 (starting page 3 of non-final office action)

The Examiner asserts:

"6. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cherubini et al (US Patent Number 6,741,551) in view of McCallister et al (US 6,005,897)." (hereinafter referred to as "Cherubini" and "McCallister", respectively)(non-final office action, Paper No./Mail Date 20080219, p. 3)

The Applicant respectfully traverses.

The Examiner also asserts:

"Cherubini et al. discloses all of the subject matter as described above except for specifically teaching encoding a plurality of information bits, thereby generating a plurality of encoding bits; rearranging an order of the plurality of encoded bits, thereby generating a sequence of discrete-valued modulation symbols.

However, McCallister et al., in the same field of endeavor, teaches encoding a plurality of information bits, thereby generating a plurality of encoding bits (52, 56, 62 in figure 3); rearranging an order of the plurality of encoded bits, thereby generating a sequence of discrete-valued modulation symbols (restructuring encoded bits by puncture controller is interpreted to be rearranging an order of the plurality of encoded bits. See figure 3 and col 7, lines 59-64) (62, 64, 68 in figure 3 and col 7, lines 59-67, col 8, lines 1-65).

One of ordinary skill in the art would have clearly recognized that in order to change a signal such as bistream into code format encoder devices are used. Encoding the data along with Trellis Coded Modulation (TCM) allows highly efficient transmission of information over communication channels. To convert the signal into bistream and output the complex symbols it would have been obvious to one ordinary skill in the art at the time the invention was made to use an encoder as taught by McCallister et al. in the Cherubini et al. system and method to provide good result during the code generation in the system. Also, it will allow the data to be transmitted over the communication channels more efficiently." (non-final office action, Paper No./Mail Date 20080219, p. 4-5, emphasis added)

The Applicant respectfully points out that although McAllister does teach and disclose a "puncture controller 64", there is no indication within the teaching and disclosure of McAllister that the order of the bits (either before the puncturing or after the puncturing) gets rearranged.

The Applicant respectfully points out that puncturing and rearranging of an order of the bits are two distinct and separate operations.

The Applicant teaches and discloses this separateness of puncturing and rearranging in the Applicant's originally filed specification (including figures and written description).

The Applicant teaches and discloses:

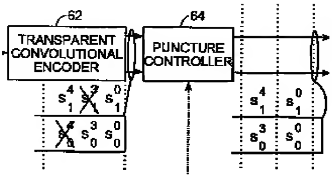
"Also, other encoding techniques may also be implemented without departing from the scope and spirit of the invention including puncturing of 1 or more of the encoded bits that are output from the encoder, rearranging the order of 1 or more of the encoded bits that are output from the encoder, and so on." (Applicant's written description, p. 26, lines 17-20)

The Applicant respectfully believes that one having skill in the art to which the invention pertains, if provided the Applicant's originally filed specification (including figures and written description), would properly understand that the puncturing and the rearranging the order are in fact two separate and distinct encoding techniques.

For example, one encoding technique is "puncturing of 1 or more of the encoded bits that are output from the encoder". Another encoding technique is "rearranging the order of 1 or more of the encoded bits that are output from the encoder".

Clearly, in accordance with the teaching and disclosure of the Applicant, both of these two distinct and separate operations (e.g., (1) puncturing and (2) rearranging the order) may be performed in a given embodiment. In such an embodiment, the "rearranging the order of 1 or more of the encoded bits that are output from the encoder" would be performed after "encoded bits … are output from the encoder". In other words, this "rearranging the order of 1 or more of the encoded bits that are output from the encoder" could be performed before performing any puncturing or after performing any puncturing.

The Applicant provides a portion of FIG. 3 of McAllister that depicts the "puncture controller 64" therein. The bits going into the "puncture controller 64" via the top path include $s_1^4 s_1^3 s_1^0$, and after the bit s_1^3 undergoes puncturing within the "puncture controller 64", the bits output there from are only $s_1^4 s_1^0$.



Similarly, the bits going into the "puncture controller 64" via the bottom path include $s_0^4 s_0^3 s_0^0$, and after the bit s_0^4 undergoes puncturing within the "puncture controller 64", the bits output there from are only $s_0^3 s_0^0$.

The Applicant respectfully points out that there is no rearranging of any order of the bits going into or out of the "puncture controller 64" in accordance with the teaching and disclosure of McAllister.

The Applicant respectfully points out that if an order of the bits $s_1^4 s_1^3 s_1^0$ was rearranged before being provided via the top path to the "puncture controller 64", then any possible combinations including ($s_1^3 s_1^4 s_1^0$, $s_1^3 s_1^0 s_1^4$, $s_1^0 s_1^3 s_1^4$, etc.) would then be provided to the "puncture controller 64". In other words, the order of the bits would be rearranged if McAllister did in fact teach and disclose this subject matter.

Moreover, the Applicant respectfully points out that if an order of the bits $s_1^4 s_1^0$ (i.e., those bits output from the top path of the "puncture controller 64") was rearranged, then an alternative possible combination would include $s_1^0 s_1^4$. In other words, the order of the bits would be rearranged if McAllister did in fact teach and disclose this subject matter.

The Applicant respectfully points out that if an order of the bits $s_0^4 s_0^3 s_0^0$ was rearranged before being provided via the bottom path to the "puncture controller 64",

then any possible combinations including ($s_0^3 s_0^4 s_0^0$, $s_0^3 s_0^0 s_0^4$, $s_0^0 s_0^3 s_0^4$, etc.) would then be provided to the "puncture controller 64". In other words, the order of the bits would be rearranged if McAllister did in fact teach and disclose this subject matter.

Moreover, the Applicant respectfully points out that if an order of the bits $s_0^3 s_0^0$ (i.e., those bits output from the bottom path of the "puncture controller 64") was rearranged, then an alternative possible combination would include $s_0^0 s_0^3$. In other words, the order of the bits would be rearranged if McAllister did in fact teach and disclose this subject matter.

The Applicant respectfully believes that McAllister does **not** teach and disclose any such rearranging of an order of the bits either going into or out of the "puncture controller 64". McAllister does teach and disclose that a bit gets punctured (i.e., deleted) within the "puncture controller 64".

However, the Applicant respectfully believes that puncturing one or more bits from a bit sequence is **not** the same as rearranging an order of the bits (either before or after one or more of them is punctured). Clearly, the Applicant teaches and discloses that these are two separate and distinct operations, as indicated by the fact that the Applicant explicitly and separately described each of these two encoding techniques (e.g., "Also, other encoding techniques may also be implemented without departing from the scope and spirit of the invention including puncturing of 1 or more of the encoded bits that are output from the encoder, rearranging the order of 1 or more of the encoded bits that are output from the encoder, and so on." as cited above).

The Applicant respectfully believes that it is clear that the Applicant teaches and discloses that two distinct and separate operations (e.g., (1) puncturing and (2) rearranging the order).

A simple sequence of 4 bits, depicted as b1, b2, b3, and b4 is employed below to show the separateness and distinction of (1) puncturing and (2) rearranging the order in various examples.

To perform puncturing ONLY of b2:

Input: b1 b2 b3 b4

Output: b1 b3 b4

To perform rearranging ONLY of an order of the bits (e.g., switching b1 and b4 in this example):

Input: b1 b2 b3 b4

Output: b4 b2 b3 b1

To perform combined puncturing of b2 as well as rearranging of an order of the bits (e.g., switching b1 and b4 in this example):

Input: b1 b2 b3 b4

Output: b4 b3 b1

The Applicant respectfully believes that the use of the term "puncturing", as employed within the art to which the invention pertains, is understood to delete, strike out, etc. one or more bits from a bit sequence or group of bits.

The Applicant respectfully believes that the term "puncturing" is not same as "rearranging an order" in accordance with the subject matter as claimed by the Applicant (e.g., as the Examiner seems to indicate by "restructuring encoded bits by puncture controller is interpreted to be rearranging an order of the plurality of encoded bits").

Again, the Applicant again respectfully believes that one having skill in the art to which the invention pertains, if provided the Applicant's originally filed specification (including figures and written description), would properly understand that the (1) puncturing and the (2) rearranging the order are in fact two separate and distinct encoding techniques.

The Applicant respectfully believes that one having skill in the art to which the invention pertains, if provided the Applicant's originally filed specification (including figures and written description), would properly understand that rearranging an order of the plurality of encoded bits would actually mean rearranging their order (i.e., switching around actual bits) and not merely puncturing one of the bits.

The Applicant respectfully asserts that merely deleting one or more bits from a group of bits (e.g., puncturing) is not the same as rearranging their order. The Applicant is unsure how an order of one of the "punctured bits" would be defined if it is no longer even there.

For example, in the Applicant's example provided above that performs "puncturing ONLY only of b2", in which the bit b2 is completed deleted from the

sequence of "b1 b2 b3 b4", the Applicant respectfully believes that the order of the bit b2 is not rearranged at all – it is merely punctured.

The order of the bits before puncturing is "b1 b2 b3 b4" and the order of the bits after puncturing is "b1 b3 b4". Before puncturing, the order of the bits is that b4 is followed by b3, which is followed by b2, which is followed by b1. It is also noted that, before puncturing, the order of the bits is that b4 is followed by b3, which is followed by b1 (with b2 in between b3 and b1).

However, after puncturing of the bit b2 (in which b2 is deleted), the order is the order of the bits is that b4 is followed by b3, which is followed by b1. Absent any rearranging of their order (which McAllister fails to teach and disclose), their relative order with respect to one another is the same before and after puncturing.

The Applicant respectfully believes that, given the fact that the Applicant explicitly teaches and discloses two distinct and separate operations (e.g., (1) puncturing and (2) rearranging the order), one having skill in the art to which the invention pertains, if provided the Applicant's originally filed specification (including figures and written description), would properly understand that puncturing does not mean rearranging the order, or vice versa.

The Applicant respectfully believes that, given the fact that the Applicant explicitly teaches and discloses two distinct and separate operations (e.g., (1) puncturing and (2) rearranging the order), one having skill in the art to which the invention pertains, if provided the Applicant's originally filed specification (including figures and written description), would properly understand that "puncturing" means "puncturing" and "rearranging the order" means "rearranging the order".

Therefore, the Applicant respectfully traverses the Examiner's apparent conclusion that "restructuring encoded bits by puncture controller is interpreted to be rearranging an order of the plurality of encoded bits" in accordance with the teaching and disclosure of McAllister.

The entuirety of the Examiner-cited portion of McAllister is provided below, and although there is teaching and disclosure therein of "puncturing", there is no indication therein of any "rearranging an order of the plurality of encoded bits" in accordance with the subject matter as claimed by the Applicant.

McAllister teaches and discloses:

"The outputs of encoder 62 provide a secondary encoded bit stream to a puncture controller 64. Puncture controller 64 selectively removes predetermined bits from the secondary encoded bit stream and appropriately restructures the secondary encoded bit stream by delaying certain encoded bits as necessary.

For the rate 7/8 example, two encoded bits are punctured out of the secondary encoded bit stream during every two unit interval period. As illustrated in FIG. 3 between vertical lines 60, during a first unit interval, puncturing does not occur. The zero-th data bit d.sub.1.sup.0 is converted by convolutional encoder 62 into encoded bits or symbols s.sub.1.sup.0 and s.sub.0.sup.0. Encoded bits s.sub.1.sup.0 and s.sub.0.sup.0 are concurrently output from puncture controller 64 during the first unit interval of a two unit interval period.

Puncturing does occur during the second unit interval of the two unit interval period. The third data bit d.sub.1.sup.3 is converted by convolutional encoder 62 into encoded bits s.sub.1.sup.3 and s.sub.0.sup.3, but encoded bit s.sub.1.sup.3 is punctured out. The fourth data bit d.sub.1.sup.4 is converted by convolutional encoder 62 into encoded bits s.sub.1.sup.4 and s.sub.0.sup.4, but encoded bit s.sub.0.sup.4 is punctured out. Encoded bit s.sub.0.sup.3 is delayed so that it is output concurrently with encoded bit s.sub.1.sup.4 from puncture controller 64 during the second unit interval of the two unit interval period. Of course, a FIFO or other rate equalizing device (not shown) may be used by convolutional encoder 62 and/or puncture controller 64 to accommodate the diverse number of encoding operations which occur in different unit intervals.

Accordingly, for the rate 7/8 embodiment, three information bits 30 are processed through convolutional encoder 62 and puncture controller 64 over a two unit interval period to produce four encoded bits or symbols. In an alternate embodiment which has no puncturing, one information bit 30 is processed through convolutional encoder 62 and puncture controller 64 during each unit interval to produce two encoded bits or symbols. Of course, in this no-puncturing embodiment, puncture controller 64 may be omitted. In other embodiments, other code rates may be achieved by extending the puncturing frame over different numbers of unit intervals to puncture different fractions of the total number of encoded bits generated by convolutional encoder 62.

So that PTCM encoder 28 can operate over a range of diverse puncturing rates, a PTCM encoder controller 66 couples to puncture controller 64 to provide a data set which defines a particular puncturing scheme to implement. In one embodiment (not shown), puncture controller 64 includes two shift registers which are loaded in parallel with a data set pattern from controller 66 and which are clocked at twice the unit interval rate so that the data set patterns circulates therein. Puncture controller 64 also includes a multiplexer coupled to the output of convolutional encoder 62 and controlled by the two shift registers. The multiplexer drives a FIFO memory. The data set patterns indicate which encoded bits to puncture out. Non-punctured encoded bits are loaded into the FIFO memory in the sequence defined by the data set and pulled out synchronously with the occurrence of unit intervals. However, those skilled in the art can devise alternate implementation techniques for puncture controller 64.

Outputs from differential encoder 54 and from puncture controller 64 couple to inputs of a mapping circuit 68. In particular, outputs from differential encoder 54 drive uncoded inputs of mapping circuit 68 and outputs from puncture controller 64 drive encoded inputs of mapping circuit 68. Two encoded bits drive encoded inputs of mapping circuit 68 in parallel during each unit interval and 2.sup.N-2 uncoded bits drive uncoded inputs of mapping circuit 68 in parallel during each unit interval, where N is the modulation order. The modulation order N equals four for the 16 P-APSK preferred embodiment depicted in FIG. 3 and equals six for the 64 P-APSK preferred embodiment. Accordingly, mapping circuit 68 maps four or more symbols per unit interval." (McAllister ,col. 7, line 59 to col. 8, line 65, emphasis added)

This Examiner-cited portion teaches and discloses "puncturing" for "appropriately restructures the secondary encoded bit stream by delaying certain encoded bits as necessary" (e.g., "Puncture controller 64 selectively removes predetermined bits from the secondary encoded bit stream and appropriately restructures the secondary encoded bit stream by delaying certain encoded bits as necessary").

In other words, some of the "predetermined bits" are selectively removed thereby "delaying certain encoded bits as necessary" to ensure proper timing considerations. This seems to be in accordance with ensuring that desired bits "concurrently output" from the "puncture controller 64" during a desired time interval.

The Applicant respectfully asserts that this teaching and disclosure of McAllister is not the same as rearranging an order of the bits (either before or after undergoing any puncturing).

The Applicant respectfully points out that McAllister could have taught and disclosed performing rearranging an order of the plurality of encoded bits (either before or after puncturing or in combination/simultaneously with the puncturing), but McAllister did not do so.

Again, the Applicant respectfully points out that although McAllister does teach and disclose a "puncture controller 64", there is no indication within the teaching and disclosure of McAllister that the order of the bits gets rearranged (either before the puncturing, after the puncturing, or in combination/simultaneously with the puncturing).

These comments made above with respect to the Examiner rejection of independent claim 1 are also applicable to independent claim 13.

Therefore, the Applicant respectfully believes that the inclusion of McAllister with Cherubini fails to overcome the deficiencies of Cherubini.

The Applicant respectfully asserts that McAllister, and Cherubini, when considered individually or together, fails to teach and disclose each and every limitation of the subject matter as claimed by the Applicant in these claims.

In view of at least these comments made above, the Applicant also respectfully believes that independent claims 1 and 13 are allowable over Cherubini in view of McAllister.

The Applicant respectfully believes that these dependent claims rejected above, being further limitations of the subject matter as claimed in allowable independent claims, respectively, are also allowable.

As such, the Applicant respectfully requests that the Examiner withdraw the rejection of these claims under 35 U.S.C. § 103(a) as being unpatentable over Cherubiniin view of McCallister.

The Applicant respectfully believes that claims 1-24 are in condition for allowance and respectfully requests that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present U.S. utility patent application.

RESPECTFULLY SUBMITTED,

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